In the Claims

1. (Currently Amended) A system for testing an integrated circuit, the integrated circuit including flip-flops connected to a logic block and the test system including:

test means operable for connecting the flip-flops as a register, and

a plurality of types of inhibition means, each type of inhibition means being operable for inhibiting one specific type of element of the logic block ~~capable of~~ having a configuration that can disturb~~ing~~ the sequencing of the register or the propagation of ~~the~~ signals into the logic block, and

control means ~~for~~ having:

a first operating mode for ~~either~~ operating the test means in synchronism with a command signal while operating continuously the inhibition means~~,~~; and

a second operating mode for ~~or~~ operating ~~any one type~~ inhibition means of a first of the plurality of types of inhibition means in synchronism with the command signal while operating continuously inhibition means of a type different than the first type and the test means, or for operating simultaneously the test means and ~~any one type~~ inhibition means of a first of the plurality of types of inhibition means in synchronism with the command signal ~~; and~~ while operating continuously ~~the other~~ inhibition means of a type different than the first type.

2. (Previously Presented) The integrated circuit test system of claim 1, wherein elements of a first type condition a clock signal provided to at least one flip-flop.

3. (Original) The integrated circuit test system of claim 2, wherein said elements of the first type include means for activating or inactivating said clock signal.

4. (Original) The integrated circuit test system of claim 1, wherein elements of a second type condition a reset signal provided to at least one flip-flop.

5. (Previously Presented) The integrated circuit test system of claim 1, wherein elements of a third type include locking elements capable of preventing the propagation of at least one signal into the logic block.

6. (Currently Amended) Scan test circuitry in an integrated circuit having a logic block including elements capable of disturbing a scan test, comprising:

a plurality of flip-flops operable as a register in a scan test mode;

inhibiting circuits for inhibiting each of the disturbing elements of the logic block from disturbing a scan test; and

a controller for ~~individually~~ successively controlling each of the inhibiting circuits individually during a scan test.

7. (Previously Presented) Scan test circuitry as defined in claim 6, wherein the controller is configured to load into the flip-flops, with all disturbing elements inhibited, a test vector for testing a first disturbing element and, subsequently, to enable the first disturbing element and to observe operation of the logic block in response to the test vector.

8. (Previously Presented) Scan test circuitry as defined in claim 7, wherein the controller is configured to scan test the first disturbing element in an active state in response to a first test vector and to scan test the first disturbing element in an inactive state in response to a second test vector.

9. (Previously Presented) Scan test circuitry as defined in claim 6, wherein the controller is configured to individually scan test each of the disturbing elements in active and inactive states.

10. (Previously Presented) Scan test circuitry as defined in claim 6, wherein the controller is configured to:

load into the flip-flops, with all disturbing elements inhibited, a first test vector for scan testing a first disturbing element in an active state;

enable the first disturbing element with all other disturbing elements inhibited;

observe operation of the logic block in response to the first test vector;

load into the flip-flops, with all disturbing elements inhibited, a second test vector for scan testing the first disturbing element in an inactive state;

enable the first disturbing element with all other disturbing elements inhibited; and

observe operation of the logic block in response to the second test vector.

11. (Previously Presented) Scan test circuitry as defined in claim 6, wherein the controller is further configured to perform a scan test with all disturbing elements inhibited by the respective inhibiting circuits.

12. (Previously Presented) Scan test circuitry as defined in claim 6, wherein at least one of the inhibiting circuits is configured to inhibit a disturbing element that affects a clock signal supplied to at least one of the flip-flops.

13. (Previously Presented) Scan test circuitry as defined in claim 6, wherein at least one of the inhibiting circuits is configured to inhibit a disturbing element that affects a reset signal supplied to at least one of the flip-flops.

14. (Previously Presented) Scan test circuitry as defined in claim 6, wherein at least one of the inhibiting circuits is configured to inhibit a disturbing element that affects at least one input from the scan test circuitry to the logic block.

15. (Previously Presented) Scan test circuitry as defined in claim 6, wherein at least one of the inhibiting circuits is configured to inhibit a disturbing element that affects at least one output of the logic block to the scan test circuitry.

16. (Currently Amended) In an integrated circuit having a plurality of flip-flops operable as a register in a scan test mode and a logic block including elements capable of disturbing a scan test, each of the elements having a type, a scan test method comprising:

(a) inhibiting all of the disturbing elements except a plurality of disturbing elements of a selected type ~~disturbing element~~;

(b) performing a scan test of the ~~selected~~ disturbing elements of the selected type;

(c) repeating steps (a) and (b) for each type of disturbing element in the logic block; ~~and~~

(d) performing a scan test of the logic block with all of the disturbing elements inhibited.

17. (Currently Amended) A scan test method as defined in claim 16, wherein performing a scan test of the selected disturbing elements comprises loading into the flip-flops a first test vector for scan testing the selected disturbing elements in an active state and observing operation of the logic block in response to the first test vector.

18. (Currently Amended) A scan test method as defined in claim 17, wherein performing a scan test of the selected disturbing elements further comprises loading into the flip-flops a second test vector for scan testing the selected disturbing elements in an inactive state and observing operation of the logic block in response to the second test vector.

19. (Currently Amended) A scan test method as defined in claim 16, wherein inhibiting all of the disturbing elements except ~~a selected~~ disturbing elements of a selected type comprises inhibiting ~~at least one~~ disturbing elements except those of a type that affects a clock signal supplied to at least one of the flip-flops.

20. (Currently Amended) A scan test method as defined in claim 16, wherein inhibiting all of the disturbing elements except ~~a selected~~ disturbing elements of a selected type comprises inhibiting ~~at least one~~ disturbing elements except those of a type that affects a reset signal supplied to at least one of the flip-flops.

21. (Currently Amended) A scan test method as defined in claim 16, wherein inhibiting all of the disturbing elements except ~~a selected~~ disturbing elements of a selected type comprises inhibiting ~~at least one~~ disturbing elements except those of a type that affects a ~~reset signal~~ locking element coupled ~~supplied~~ to at least one of the flip-flops.

22. (Currently Amended) A scan test method as defined in claim 16, wherein inhibiting all of the disturbing elements except ~~a selected~~ disturbing elements of a selected type comprises inhibiting ~~at least one~~ disturbing elements except those of a type that affects an input to the logic block from at least one of the flip-flops.

23. (Currently amended) A scan test ~~A~~ method as defined in claim 16, wherein inhibiting all of the disturbing elements except ~~a selected~~ disturbing elements of a selected type comprises inhibiting ~~at least one~~ disturbing elements except those of a type that affects an output of the logic block to at least one of the flip-flops.

24. (Currently Amended) A scan test method as defined in claim 16, wherein performing a scan test of ~~the selected~~ disturbing elements of a selected type comprises inhibiting the selected disturbing elements to load a test vector into the flip-flops and enabling the selected disturbing element to observe operation of the logic block in response to the test vector.

25. (Currently Amended) A scan test method as defined in claim 16, wherein performing a scan test of the selected disturbing elements comprises scan testing the selected disturbing elements in active and inactive states.

26. (Previously Presented) A scan test method as defined in claim 16, wherein performing a scan test of the selected disturbing element comprises:

loading into the flip-flops, with all disturbing elements inhibited, a first test vector for scan testing a first disturbing element in an active state;

enabling the first disturbing element with all other disturbing elements inhibited;

observing operation of the logic block in response to the first test vector;

loading into the flip-flops, with all disturbing elements inhibited, a second test vector for scan testing the first disturbing element in an inactive state;

enabling the first disturbing element with all other disturbing elements inhibited; and

observing operation of the logic block in response to the second test vector.